UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/813,042	03/19/2001	Li T. Wang	062891.0520	1363

7590 05/27/2005

Barton E. Showalter
Baker Botts L.L.P.
2001 Ross Avenue, Suite 600
Dallas, TX 75201-2980

EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/813,042	Applicant(s) WANG, LI T.	
	Examiner Khanh Tran	Art Unit 2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-21* is/are allowed.

6)☒ Claim(s) *1-3,6,8-11,13,15 and 17* is/are rejected.

7)☒ Claim(s) *4,5,7,12,14,16 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/08/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 12/08/2004 has been entered. Claims 1-21 are pending in this Office action.

Response to Arguments

2. Applicant's arguments with respect to claims 1-3, 8-9, 10, 15 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claim 6 is objected to because of the following informalities: Claim 6 is objected for lack of antecedent basis because claim 6 recites the first amplifier and the second amplifier, which claim 1 does not recite. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Choi U.S. Patent 5,767,696.

Regarding claim 1, in column 1 line 60 via column 2 line 15, Choi discusses a tri-state device of figure 2 prior art. Referring to Table 2, see also figure 2, the tri-state device includes:

A first input data signal, node A;

A second input data signal, node B.

When input A is logic zero, output Y goes to logic 0, corresponding to the claimed first state.

When input A is logic one, output Y enters a floating state, corresponding to the claimed second state.

When input A is logic one and input B is a logic one, output Y goes to logic 1, corresponding to the claimed third state.

Regarding claim 3, when input A is logic one and input B is logic 0, output Y enters a floating state. NMOS transistor MN1 and NMOS transistor MN2 form an amplifier. Because NMOS transistor MN1 is off, output of NMOS transistor MN1 is coupled to the data line into an open drain state.

Regarding claim 15, claim 15 is rejected on the same ground as for claim 1 because of similar scope.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi U.S. Patent 5,767,696.

Regarding claim 2, referring to figure 2, the tri-state device employs a pull-up resistor PR coupled to the data line; in column 1 line 60 via column 2 line 15. When output Y goes to logic 0 as discussed above, the output signal INA is equal to VSS. However, Choi does not teach VSS is 0 voltage. Nevertheless, a person of average skill in the art would have recognized that a voltage 0 would correspond to a logical 0, therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention that the voltage VSS can be modified to be close to 0-voltage value. In view of the modification, output Y is pulled close to zero voltage level as claimed.

Regarding claim 8, claim 8 is rejected on the same ground as for claim 1 because similar scope. Admitted figure 2 prior art does not teach a first amplifier and second amplifier. Nevertheless, as known in the art of amplifier technology, amplifier can be constructed using transistors. In view of the foregoing reasoning, one of ordinary skill in the art would have recognized that PMOS transistors MP1 MP2 form a first amplifier and NMOS transistors MN1 MN2 form a second amplifier.

Regarding claim 9, claim 9 is rejected on the same ground as for claim 2 because of similar scope.

Regarding claim 10, when input A is logic one and input B is logic 0, output Y enters a floating state, corresponding to the claimed second state as recited in claim 1. Because PMOS transistor MP1 is off, PMOS transistor MP1 establishes an open drain state for PMOS transistor MP1 and PMOS transistor MP2.

Regarding claim 11, when input A is logic one and input B is logic one, output Y goes to a logical one, corresponding to the claimed third state as recited in claim 1. Because PMOS transistor MP1 is off, PMOS transistor MP1 establishes an open drain state for PMOS transistor MP1 and PMOS transistor MP2.

5. Claims 6, 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi U.S. Patent 5,767,696 in view of admitted prior art.

Regarding claim 6, referring to figure 2 of Choi invention, PMOS transistors MP1 MP2 form a first amplifier and NMOS transistors MN1 MN2 form a second amplifier as appreciated by one of ordinary skill in the art.

Choi, however, does not teach the first amplifier and second amplifier being an open drain GTL (Gunning Transceiver Logic) buffer and SSTL (Stub Series Terminated Logic) as set forth in the application claim.

Nevertheless, as disclosed in Background of the Invention of the original disclosure, Applicant admits several binary logic standards such as Gunning Transceiver Logic (GTL) and Stub Series Terminated Logic (SSTL) defining the different voltage levels and timing requirements to allow receivers to resolve the logic zero and logic one signals. In view of that, it would have been obvious for one of ordinary skill in the art at the time of the invention that admitted figure 2 prior art of Choi invention can be modified to use the recited logic standards. The modification is obvious because the logic standards would precisely define different voltage levels and timing requirements, which are very important in a logical circuit.

Regarding claims 13 and 17, claims 13 and 17 are rejected on the same ground as for claim 6 because of similar scope.

Allowable Subject Matter

6. Claims 4-5, 7, 12, 14, 16, 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 19-21 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 19, claim 19 is allowable over prior art of record since the cited references taken individually or in combination fails to particularly disclose a communication server comprising all elements as set forth in the claimed invention.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Priel U.S. Patent 3,792,292 discloses "Three-State Logic Circuit".

Ganapathy et al. U.S. Patent 6,446,195 discloses "Dyadic Operations Instruction Processor With Configurable Functional Blocks".

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

Khanh Cong Tran 05/26/2005

Examiner KHANH TRAN